Remarks

In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

The non-final Office Action dated June 4, 2008, lists the following objections and rejections: an objection to the drawings; an objection to the title of the invention; objections to claims 1-25; and claims 1-25 stand rejected under 35 U.S.C. § 102(e) over Corbin *et al.* (U.S. Patent No. 7,103,814).

In response to the objection to the title of the invention, Applicant has amended the title in a manner consistent with that suggested by the Examiner as is indicated on page 2 of this paper. Thus, Applicant requests that the objection to the title be removed.

In response to the objection to the drawings, Applicant has labeled Figures 1, 2A, 2B, 3A and 3B as prior art as requested by the Examiner as is indicated on page 3 of this paper. Thus, Applicant requests that the objection to the drawings be removed.

Applicant respectfully traverses the objections to claims 1-25 because the various aspects of these claims would be clear to the skilled based on Applicant's disclosure. Notwithstanding, in an effort to facilitate prosecution, Applicant has amended certain claims (*e.g.,* claim 1) in manner consistent with that which was suggested by the Examiner and Applicant has removed the expression "such that" from claims 13 and 23. Regarding aspects of claims 10 and 23 directed to a pipelined manner, Applicant submits that these aspects would be clear to the skilled artisan based on Applicant's specification. *See, e.g.,* paragraph 0048. Thus, Applicant requests that the objections to claims 1-25 be withdrawn.

Applicant respectfully traverses the § 102(e) rejection of claims 1-25 because the cited portions of Corbin do not correspond to the claimed invention which includes, for example, aspects directed to a global enable signal that places the modules in a test mode (*see, e.g.,* claims 1-12) and testing the module in response to a global enable signal being activated (*see, e.g.,* claims 13-25). The Office Action asserts that Corbin's "scan test enable" corresponds to the global enable signal of the claimed invention. The cited portions of Corbin, however, do not mention any "scan test enable" or any "scan test enable signal". In fact a word search of Corbin fails to reveal any mention of a "scan test enable" or a "scan test enable signal". As such, the Office Action fails to assert

correspondence between the Corbin reference and each aspects of the claimed invention as required. Accordingly, the § 102(e) rejection of claims 1-25 is improper and Applicant requests that it be withdrawn. In an effort to facilitate prosecution, Applicant has reviewed the cited portions of Corbin, and Applicant submits that Corbin does not teach or suggest a global enable signal that places the modules in a test mode as in the claimed invention. Should any rejection based on the Corbin reference be maintained, Applicant requests clarification regarding how Corbin is being asserted as teaching a global enable signal as in the claimed invention. In view of the need for such clarification, Applicant should also be afforded an opportunity to respond prior to a final rejection pursuant to M.P.E.P. § 706.07 ("Before final rejection is in order a clear issue should be developed between the examiner and applicant.").

Applicant further traverses that the § 102(e) rejection of claims 1-12 and 14-22 because the cited portions of Corbin do not correspond to aspects of the claimed invention directed to a control circuit that controls whether or not the global enable signal is passed to an associated module. The Office Action erroneously asserts that Corbin's general purpose test latch 40 corresponds to Applicant's control circuit. Instead, the cited portions of Corbin teach that latch 40 provides a control signal that puts MUX 50 into a bypass mode by selecting the scan IN signal instead of the output 44 of the BIST engine, which allows logic patterns to be loaded and results unloaded via the scan chains while the BIST engine is running. *See, e.g.,* Figure 2 and Col. 3:30-47. Corbin's latch 40 simply provides a bypass signal that is used to bypass the BIST engine. Applicant submits that Corbin's latch 40 does not receive a global enable signal that places the modules in a test mode and Corbin's latch 40 does not control the passing of any global enable signal to the modules. As such, Corbin's latch 40 does not correspond to Applicant's control circuit. Accordingly, the § 102(e) rejection of claims 1-12 and 14-22 is improper and Applicant requests that it be withdrawn.

Applicant further traverses that the § 102(e) rejection of claims 2-4 and 15-17 because the Office Action's assertion of correspondence between the cited portions of Corbin and the claimed invention is illogical. The claimed invention requires that the control circuit be controlled by a dedicated bypass signal. The cited portions of Corbin, however, teach that the latch 40 provides the bypass signal instead of being controlled by

the bypass signal. Moreover, Applicant traverses the Office Action's assertion that Corbin discloses that latch 40 "receives the scan test enable signal". Applicant submits that the cited portions of Corbin do not mention any such teachings. *See, e.g.,* Figure 2 and Col. 3:30-47. In fact, Corbin fails to make any mention of a scan test enable or a scan test enable signal as discussed above. Accordingly, the § 102(e) rejection of claims 2-4 and 15-17 is improper and Applicant requests that it be withdrawn.

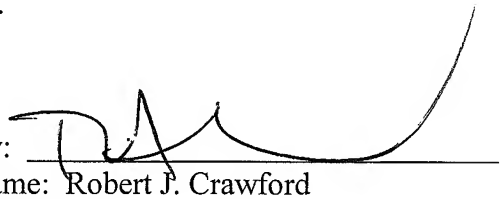
Applicant further traverses that the § 102(e) rejection of claims 13-25 because the cited portions of Corbin do not correspond to aspects of the claimed invention directed to placing the other modules in a transport mode of operation while testing the module. The cited portions of Corbin do not teach that scan IN and Scan OUT chains are placed in a transport mode of operation while the BIST engine is being tested. *See, e.g.,* Figure 2 and Col. 3:30-47. Instead, Corbin teaches that logic testing also takes place while the memory is tested; for example, logic test patterns are loaded and test results are unloaded via the scan chains while the memory is being tested *See, e.g.,* Col. 3:23-33. As such, the cited portions of Corbin do not teach placing any modules in a transport mode of operation while testing the module. Accordingly, the § 102(e) rejection of claims 13-25 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: 
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633
(NXPS.558PA)

Attachments: Five replacement drawing sheets